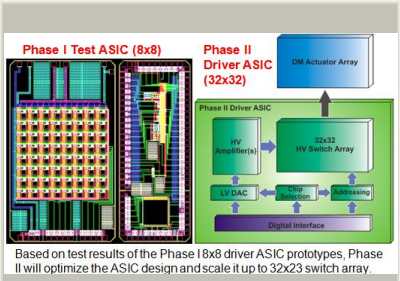
Driver ASICs for Advanced Deformable Mirrors, Phase II

Completed Technology Project (2014 - 2016)

Project Introduction

The overall goal of the SBIR program is to develop a new Application Specified Integrated Circuit (ASIC) driver to be used in driver electronics of a deformable mirror (DM) system in order to reduce power dissipation, improve controllability, enhance preciseness, and to significantly reduce the form factors of the entire DM system, thus making it suitable for space-based deployment. A unique capability is being enabled through this SBIR program that allows selection from various DM vendors a best DM to be integrated with the driver ASIC in order to build an extremely high contrast, compact, and low-mass coronagraphs and nulling interferometer system onto a space-based telescope. Given its superior performances namely (1) low power dissipation, (2) high control preciseness, (3) tiny chip estate and low mass, (4) minimal number of needed cables, and (5) universal capability in driving various piezoelectric actuator loads, the proposed ASIC driver technology holds the promise of enabling ultimate deployment of low power, low payload, low cost, and high-performance adaptive optics (AO) systems into NASA's space-based platforms. The feasibility of the proposed Phase II approach is demonstrated through eight major technical objectives: (1)packaging and characterizations of the Phase I 8x8 driver ASIC, and based on the test results, (2) design optimization and simulation of the Phase II 32x32 switch array driver ASIC, (3) layout, simulation verification, and tape out for ASIC manufacturing, (4) packaging and basic characterizations of the driver ASIC, (5) ASIC UBM (Under Ball Metallurgy) fabrication, (6) building ASIC PC communication interface and PC software development, (7) fabrication of capacitive load arrays made of different piezoelectric materials, and (8) characterizations of the final Phase II 32x32 switch array driver ASIC in integration with load/actuator arrays.



Based on test results of the Phase I 8x8 driver ASIC prototypes, Phase II will optimize the ASIC design and scale it up to 32x23 switch array.

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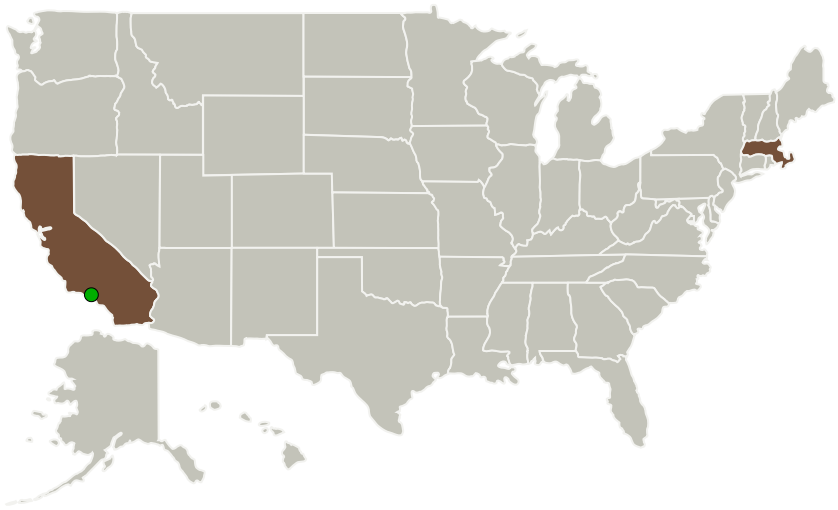
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Microscale, Inc.	Lead Organization	Industry Small Disadvantaged Business (SDB)	Woburn, Massachusetts
Jet Propulsion Laboratory(JPL)	Supporting Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations	
California	Massachusetts

Project Transitions

April 2014: Project Start

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Microscale, Inc.

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

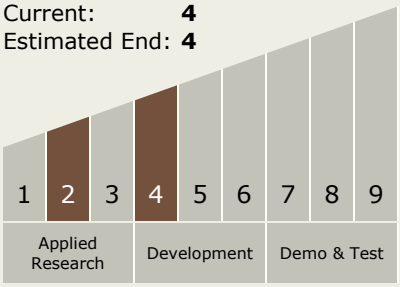
Carlos Torrez

Principal Investigator:

Xingtao Wu

Technology Maturity (TRL)

Start: **2**
Current: **4**
Estimated End: **4**



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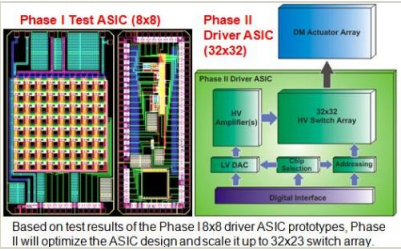
April 2016: Closed out

Closeout Summary: Driver ASICs for Advanced Deformable Mirrors, Phase II P roject Image

Closeout Documentation:

- Final Summary Chart Image*(https://techport.nasa.gov/file/137467)*

Images



Briefing Chart Image
Driver ASICs for Advanced Deformable Mirrors, Phase II *(https://techport.nasa.gov/image/130998)*

Technology Areas

Primary:

- TX08 Sensors and Instruments
  - TX08.2 Observatories
    - TX08.2.1 Mirror Systems

Target Destinations

The Moon, Mars, Outside the Solar System, The Sun, Earth, Others Inside the Solar System